

Digital Step Attenuator

- 1dB steps to 31dB
- Parallel (P) or Serial (S) programming
- Positive CMOS control logic
-

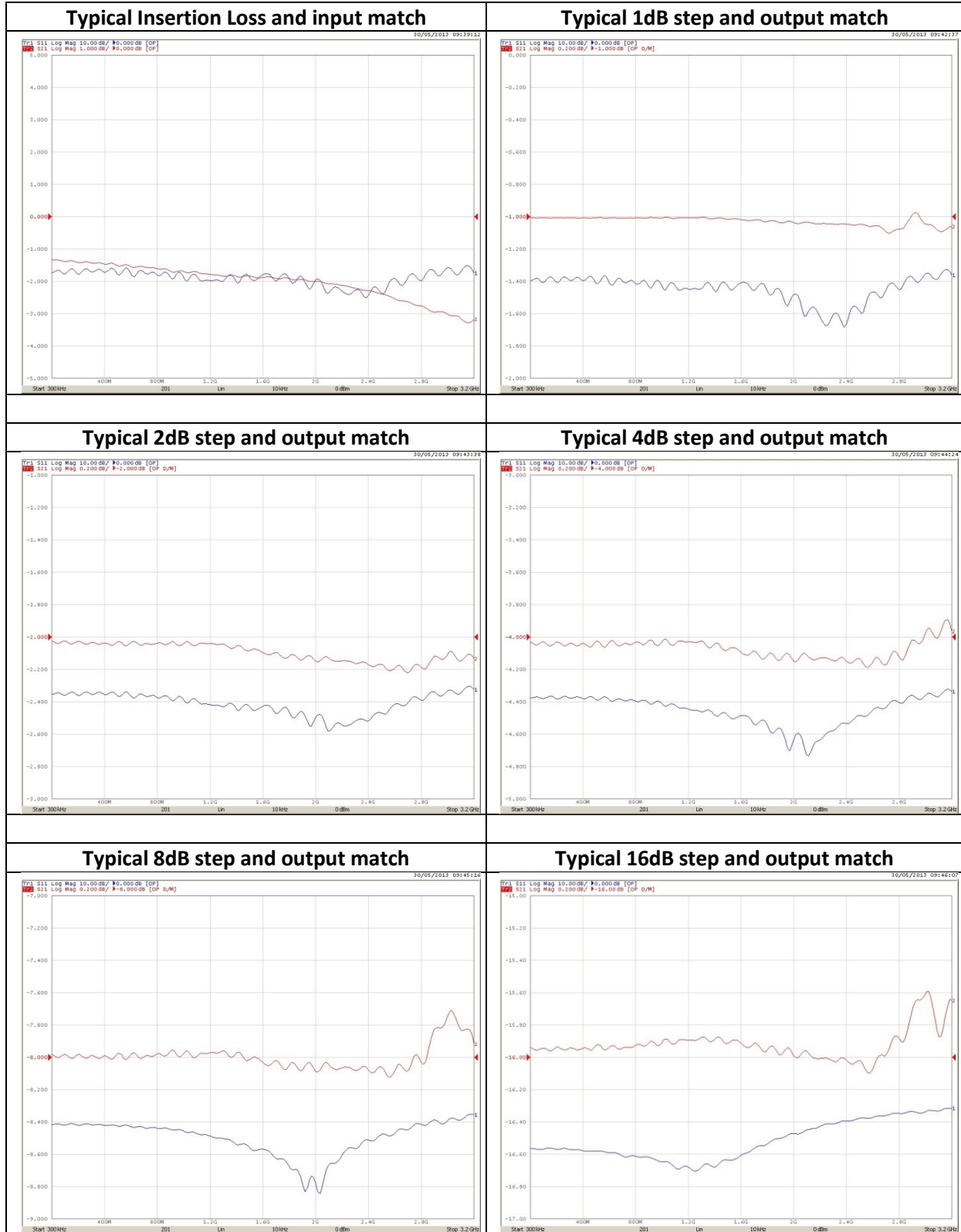
Applications:

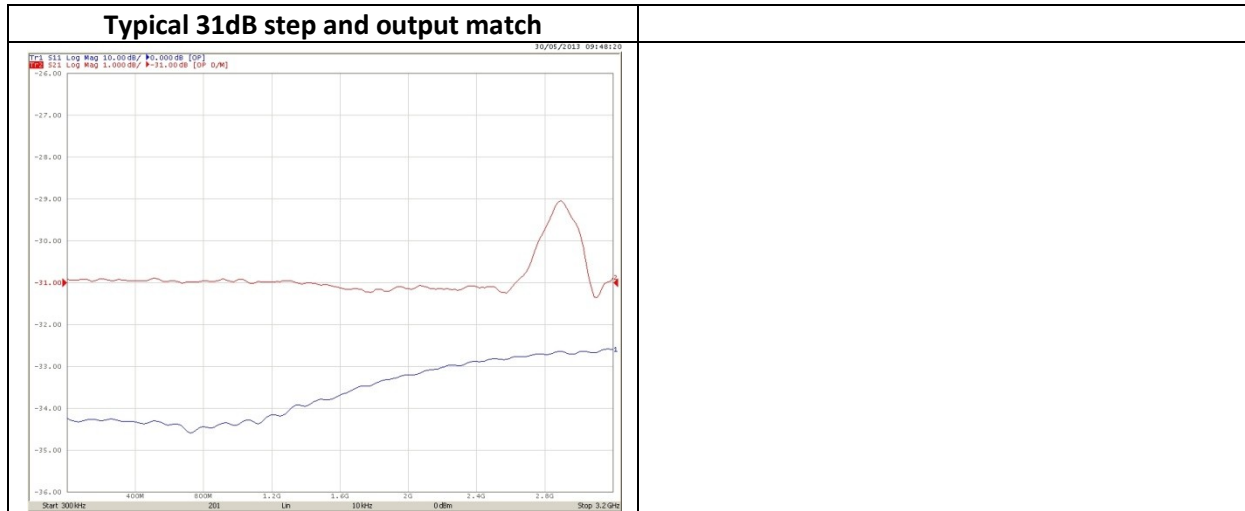
- Automated test bench
- Lab
- Telecom



| | Unit | Min | Typ. | Max. | |
|----------------------------|------|---------------------|-----------|------|----------------|
| Bandwidth | MHz | 1 | | 3200 | |
| Insertion Loss | dB | | 1.7 | | |
| Accuracy | dB | | ±(0.3+3%) | | |
| P1dB: | dBm | | +30 | | |
| IIP3: | dBm | | 50 | | 2 tones +18dBm |
| Return Loss | dB | | 18 | | |
| Switching speed | μs | | | 1.0 | |
| Max Input power | dBm | | | +27 | |
| Current sink | mA | | 10 | | |
| Power supply | V | 5 | | 15 | |
| Control voltage (S or P) | V | | 5 | | |
| Operating case temperature | °C | -40 | | +85 | |
| Storage temperature | °C | -55 | | +100 | |
| Dimensions | | See outline drawing | | | |
| Weight | g | | 85 | | |

Measured at 25°C, in a 50Ω system at room temperature unless otherwise specified





Serial programming (AAT3200-31-S):

The **AAT3200-31-S** is a 5-bit controlled Digital Step Attenuator (DSA).
It is controlled by 3 CMOS compatible signals :

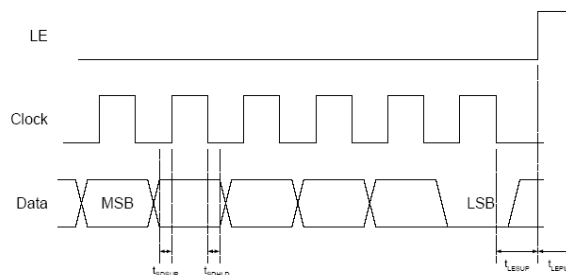
- Data
- Clock
- Latch Enable (LE)

The LE input controls the latch.

When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator.

When LE is brought LOW, data in the shift register is latched.

- Serial interface timing diagram



- Register map

| | | | | | |
|-----------|-----------|-----------|-----------|-----------|-----------|
| B5 | B4 | B3 | B2 | B1 | B0 |
| C16 | C8 | C4 | C2 | C1 | 0 |

↑
MSB (first in)

↑
LSB (last in)

B0 must always be « 0 » in order to avoid unwanted states

➤ Serial interface characteristics

| Symbol | Parameter | Min | Max | Unit |
|-------------|--|-----|-----|------|
| f_{CIK} | Serial data clock frequency (Note 1) | | 10 | MHz |
| t_{CIKH} | Serial clock HIGH time | 30 | | ns |
| t_{CIKL} | Serial clock LOW time | 30 | | ns |
| t_{LESUP} | LE set-up time after last clock falling edge | 10 | | ns |
| t_{LEPW} | LE minimum pulse width | 30 | | ns |
| t_{SDSUP} | Serial data set-up time before clock rising edge | 10 | | ns |
| t_{SDHLD} | Serial data hold time after clock falling edge | 10 | | ns |

➤ Pinout

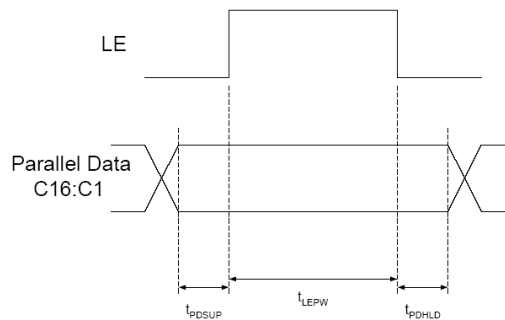
TBD

Parallel Programming (AAT3200-31-P) :

The **ATT3200-31-P** is a 5-bit controlled Digital Step Attenuator (DSA).

For parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 18) to latch new attenuation state into device.

➤ Parallel interface timing diagram



➤ Truth table

| C16 | C8 | C4 | C2 | C1 | Attenuation State |
|-----|----|----|----|----|-------------------|
| 0 | 0 | 0 | 0 | 0 | Reference Loss |
| 0 | 0 | 0 | 0 | 1 | 1 dB |
| 0 | 0 | 0 | 1 | 0 | 2 dB |
| 0 | 0 | 1 | 0 | 0 | 4 dB |
| 0 | 1 | 0 | 0 | 0 | 8 dB |
| 1 | 0 | 0 | 0 | 0 | 16 dB |
| 1 | 1 | 1 | 1 | 1 | 31 dB |

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➤ Parallel interface characteristics

| Symbol | Parameter | Min | Max | Unit |
|-------------|---|-----|-----|------|
| t_{LEPW} | LE minimum pulse width | 10 | | ns |
| t_{PDSUP} | Data set-up time before rising edge of LE | 10 | | ns |
| t_{PDHLD} | Data hold time after falling edge of LE | 10 | | ns |

➤ Pinout

TBD

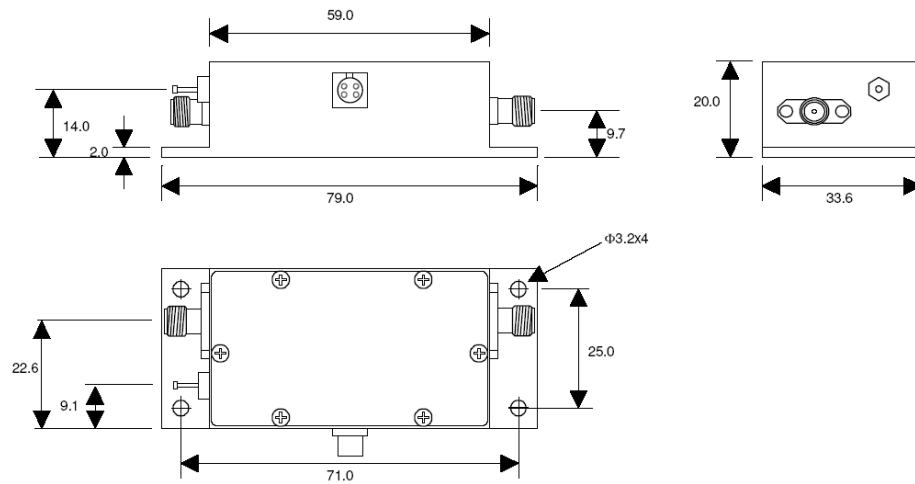
Other interface :

Upon special request, an USB, RS232 or RS285 interface can be implemented. Contact the factory

AAT3200-31-S/P

Outline Drawing

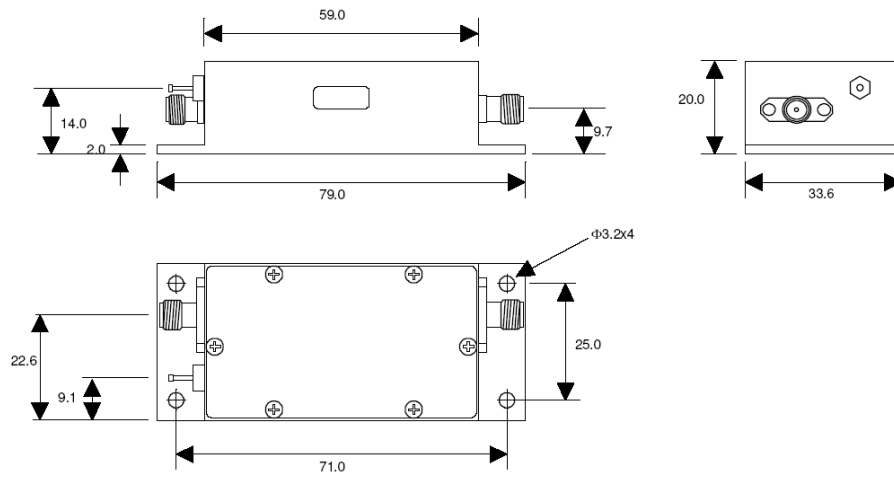
ATT3200-31-S



Finishing: Nickel-plated (except connectors)
 All dimensions in mm
 Tolerance: +/-0.1mm

ATT3200-31-P

AAT3200-31-S/P



Finishing: Nickel-plated (except connectors)
All dimensions in mm
Tolerance: +/-0.1mm